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EXAMINER	
TRAN, KHANH C	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,826	MAGEE, DAVID PATRICK	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-21,23,24 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-11,14-21,23,24 and 26-29* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 07/12/2005 has been entered. Claims 1-6, 8-21, 23-24 and 26-29 are pending in this Office action.

Response to Arguments

2. Applicant's arguments with respect to claims 1-6, 8-10, 14-21, 23-24 and 26-29 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 10-11, 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luo et al. U.S. Patent 5,481,488.

Regarding claim 1, in column 1 line 15 via column 2 line 45, Luo et al. discusses an FFT butterfly processor for arithmetic operation. The block floating point algorithm is widely used in butterfly computation due to its high-speed processing for blocked data. As described above, the butterfly unit includes several multiply, add, and subtract operations, and thus an increase of data range may occur, resulting in an overflow. However, in general the butterfly processor is made up of fixed-point multipliers and

adders. Therefore, guard bits must be provided in the butterfly processor to prevent an overflow error occurring in the computational result of a certain butterfly computation.

The butterfly computation of the 8-point FFT is performed by three butterfly stages I, II, and III, and each stage includes four butterfly units, as shown in FIG. 2. The computational requirements of one butterfly unit are one complex multiply, one complex add, and one complex subtract. As is known, these complex computations have to be changed into real computations, including three real additions, three real subtractions, and four real multiplications. Luo et al. further discusses that since the butterfly units in the same butterfly stage have different data inputs, the overflow bit number a computational result may be different in each different butterfly unit.

In view of that, in the first butterfly unit of the first stage of 8-point FFT, a first summation for N points of the 8-point FFT is performed to determine the total of bits overflowed.

A second summation is performed on another butterfly unit to determine the number of bits overflowed.

Luo et al. does not disclose the comparison step as set forth in the application claim. However, Luo et al. further discloses that the overflows of all resultant data from the butterfly units in the same stage have to be detected to obtain the largest overflow bit number. Because the overflows of all resultant data from the butterfly units in the same stage have to be detected, it would have been obvious for one of ordinary skill in the art at the time of the invention that the conventional mechanism for performing FFT

butterfly computation can be modified to compare the overflow bits of all the butterfly units in the same stage in order to determine appropriate scaling.

Regarding claim 2, as recited in claim 1, the computational requirements of one butterfly unit are one complex multiply, one complex add, and one complex subtract. Hence, the butterfly units in the same stage require a plurality of complex additions and complex multiplications.

Regarding claim 3, in column 1, lines 15-30, Luo et al. further discusses that the FFT butterfly computation operates on data in sets of r points, where r is called the radix. A P-point FFT uses P/r butterfly units per stage for $\log_r P$ stages. The computational result of one butterfly stage is the input data of the next butterfly stage.

Regarding claim 4, in column 1, lines 15-30, Luo et al. discusses an example in figure 1 a signal flow diagram of a basic radix-2 butterfly unit is illustrated in FIG. 1, and a signal flow diagram of an 8-point radix-2 FFT processor is illustrated in FIG. 2.

Regarding claim 5, as recited in claim 1, the overflows of all resultant data from the butterfly units in the same stage have to be detected to obtain the largest overflow bit number. In column 2, lines 1-5, the resultant data have to be shifted by the largest overflow bits before entering the next-stage butterfly computation. The overflow in each stage corresponds to the claimed bit growth.

Regarding claim 6, in column 1 line 55 via column 2 line 10, Luo et al. discusses that since the butterfly units in the same butterfly stage have different data inputs, the overflow bit number a computational result may be different in each different butterfly unit. For example, two-bit overflow, one-bit overflow, or non-overflow may happen in a radix-2 butterfly unit. Because all decimal points of the computing data in every one butterfly stage have to be aligned when the fixed-point butterfly processor is used, these different overflows cannot be shifted individually by different bits. Therefore, the overflows of all resultant data from the butterfly units in the same stage have to be detected to obtain the largest overflow bit number. These resultant data have to be shifted by the largest overflow bits before entering the next-stage butterfly computation. If non-overflow occurs, shifting, corresponding to the claimed scaling, is omitted as appreciated by one of ordinary skill in the art.

Regarding claim 10, claim 10 is rejected on the same ground as for claim 3 in view of claim 4 because of similar scope.

Regarding claim 11, claim 11 is rejected on the same ground as for claim 3 in view of claim 4 because of similar scope. As recited in claim 3, a P-point FFT uses P/r butterfly units per stage for $\log_r P$ stages. In view of that, a 128-point FFT uses $\log_r 128$ stages as appreciated by one of ordinary skill in the art.

Regarding claim 23, as recited in claim 1, Luo et al. discusses an FFT butterfly processor for arithmetic operation. As described above, the butterfly unit includes several multiply, add, and subtract operations, and thus an increase of data range may occur, resulting in an overflow. However, in general the butterfly processor is made up of fixed-point multipliers and adders. Therefore, guard bits must be provided in the butterfly processor to prevent an overflow error occurring in the computational result of a certain butterfly computation.

The butterfly computation of the 8-point FFT is performed by three butterfly stages I, II, and III, and each stage includes four butterfly units, as shown in FIG. 2. The computational requirements of one butterfly unit are one complex multiply, one complex add, and one complex subtract. As is known, these complex computations have to be changed into real computations, including three real additions, three real subtractions, and four real multiplications. Luo et al. further discusses that since the butterfly units in the same butterfly stage have different data inputs, the overflow bit number a computational result may be different in each different butterfly unit.

In view of that, in the first butterfly unit of the first stage of 8-point FFT, a first summation for N points of the 8-point FFT is performed to determine the total of bits overflowed.

A second summation is performed on another butterfly unit to determine the number of bits overflowed.

Luo et al. does not discuss the comparison step as set forth in the application claim. However, Luo et al. further discusses that the overflows of all resultant data from

the butterfly units in the same stage have to be detected to obtain the largest overflow bit number. Because the overflows of all resultant data from the butterfly units in the same stage have to be detected, it would have been obvious for one of ordinary skill in the art at the time of the invention that the conventional mechanism for performing FFT butterfly computation can be modified to compare the overflow bits of all the butterfly units in the same stage in order to determine appropriate scaling.

Regarding claim 24, claim 24 is rejected on the same ground as for calim 6 because of similar scope.

4. Claims 8-9, 14-15 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vandenameele-Lepla US Patent Publication 2003/0058787 A1 in view of Williams U.S. Patent 5,717,620.

Regarding claim 8, in paragraph [0013], Vandenameele-Lepla teaches that in multi-carrier data communication systems such as OFDM, channel equalization is accomplished by first estimating and then compensating for the channel frequency response at the receiver end.

In paragraph [0006], Vandenameele-Lepla teaches that a subset of the plurality of time-domain signals includes training symbols that are embedded into the data for channel estimation purposes. In paragraph [0007], a correlator received the training sequence embedded in the multi-carrier time domain-signal

by correlation process. In view of that, the correlator would perform an equivalent function of the claimed training tone extractor.

In paragraph [0013], an initial set of frequency-domain channel estimates are derived by dividing the received frequency-domain signals by their corresponding frequency domain training symbols. The initial frequency-domain channel estimates go through an IFFT and are transformed into time domain.

A weighting matrix that accounts for the finite time response of the channel and the position of the sub-carriers in the frequency domain is then processed in time domain to determine the maximum likelihood time domain estimates. This is then followed by an FFT to produce frequency domain channel estimates with reduced noise that are fed back to the equalizer.

Vandenameele-Lepla does not teach a channel estimator comprising the elements discussed above as claimed in the application claim. Since Vandenameele-Lepla teaches the method for channel equalization performing the aforementioned steps, one of ordinary skill in the art that at the time of the invention would have been motivated to implement a channel estimator including all components as discussed above.

Vandenameele-Lepla does not teach a Fast Fourier Transform component as set forth in the application claim. Nevertheless, the Fast Fourier Transform component is discussed in claim 1 rejection in view of a conventional FFT butterfly processor. Because Vandenameele-Lepla teachings, employing a Fast Fourier Transform, result in significant reduction in complexity in channel

equalization, therefore, it would have been obvious for one of ordinary skill in the art that at the time of the invention that Vandenameele-Lepla FFT can be modified to implement the Fourier transform butterfly circuits as discussed in Luo et al. invention. The modification is obvious because the FFT butterfly circuit performs a reduced Fast Fourier Transform with processing stages that compensates for bit overflows and Vandenameele-Lepla teachings result in significant reduction in computational complexity.

Regarding claim 9, claim 9 is rejected on the same ground as for claim 8 and further in view of claim 1 because of similar scope.

Regarding claim 14, Vandenameele-Lepla teachings apply to multi-carrier data communication systems such as OFDM.

Regarding claim 15, in column 1, lines 9-26, as discussed in Williams invention, it becomes practical to employ digital signal processing for channelizing a wide-band radio signal for de-multiplexing multiple frequency-division-multiplexed channels by fast-Fourier transformation. In light of that, one of ordinary skill in the art would have been motivated to include the butterfly circuit as shown in figure 4 as part of a digital signal processing chip.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 27, claim 27 is rejected on the same ground as for claim 9 and further in view of claim 1 because of similar scope.

Regarding claim 28, Vandenameele-Lepla teachings apply to multi-carrier data communication systems such as OFDM and the channel impulse response has a finite duration impulse response as appreciated by one of ordinary skill in the art.

Regarding claim 29, claim 29 is rejected on the same ground as for claim 6 because of similar scope.

5. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams U.S. Patent 5,717,620 in view of Luo et al. U.S. Patent 5,481,488.

Regarding claim 16, claim 16 is rejected on the same ground as for claim 1 because similar scope.

Williams does not discuss a modem as set forth in the application claim. As disclosed in Williams U.S. Patent 5,717,620, the receiver includes a wide-band digital tuner 12, which corresponds to the claimed front-end portion for receiving data encoded in time domain, and a channelizer 16 which takes the form of fast Fourier transform butterfly circuit as disclosed in figure 4. Hence,

channelizer 16 corresponds to the claimed digital signal processor. The butterfly circuit shown in figure 4 further includes a bit growth detector 39 for monitoring the inputs to the inter-pass memory 32 so as to keep track of the largest value applied during any given pass; see column 2 line 65 via column 5 line 15. In view of that, the step of monitoring the inputs to the inter-pass memory 32 corresponds to the claimed step of "analyzing the general consistent format of the time domain data signals".

Williams, however, does not teach a modem comprising elements as set forth in the application claim. Nevertheless, as well known in the art, modem is a transceiver and the base station as discussed in figure 1 of Williams is also a transceiver. In view of that, it would have been obvious for one of ordinary skill in the art at the time of invention that the teachings of figure 1 can be modified to apply to a modem as claimed in the application claim. Furthermore, Williams teachings employ fast Fourier transform butterfly circuit for detecting correcting the bit growth during Fourier transform computations, therefore, it would have been obvious for one of ordinary skill in the art at the time of invention that Williams teachings can be modified to include the conventional FFT butterfly processor as discussed in Luo et al. invention. As discussed in claim 1, the overflows of all resultant data from the butterfly units in the same stage are detected to obtain the largest overflow bit number. These resultant data have to be shifted by the largest overflow bits before entering the next-stage butterfly computation.

Regarding claim 17, as discussed in column 4, lines 20-35 of Williams invention, the design of prior art figure 2 is to maximize accuracy by using bit shifting to take advantage of as many of the circuit's bit position as possible. Because designing a circuit would involve in modeling and simulation, one of ordinary skill in the art will recognize that prior art teachings would model and simulate the format input before actually implement the butterfly circuit.

Regarding claim 18, as discussed in Luo et al. invention, the overflows of all resultant data from the butterfly units in the same stage are detected to obtain the largest overflow bit number. In view of the foregoing, the overflow of each individual butterfly unit is detected and stored.

Regarding claim 19, the base station in figure 1 of Williams invention is a wireless base station.

Regarding claim 20, claim 20 is rejected on the same ground as for claim 16 because of similar scope. Furthermore, as shown in figure 1 of Williams invention, a receiver includes a wideband digital tuner 12 for receiving digitized signals in time domain, a digital channelizer for digital signal processing for channelizing a wideband digital signal for de-multiplexing multiple frequency-division multiplexed channels by fast Fourier transformation implemented as a butterfly circuit discussed in Luo et al. invention.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 6 because of similar scope.

Allowable Subject Matter

6. Claims 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Naveh et al. U.S. Patent 6,411,978 B1 disclose "Mechanism For Block Floating Point FFT Hardware Support On A Fixed Point Digital Signal Processor".

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 09/29/2005

Examiner KHANH TRAN